REMARKS/ARGUMENT

Claims 9-22 are now presented for examination. Claims 9 and 20 are the only independent claims.

Claim 20 was rejected under 35 U.S.C. § 102(b) as anticipated by U.S. Patent 5,668,755 (Hidaka et al.). Claims 9-15, 19 and 22 were rejected under 35 U.S.C. § 103 as obvious from Hidaka et al. in view of U.S. Patent 5,571,735 (Mogami et al.). Applicant submits that independent claims 9 and 20 are patentable over the cited prior art for at least the following reasons.

As was discussed in the previous response, an inversion bias applied to a gate electrode of a MOS structure causes the growth of a depletion region in the semiconductor channel region from the interface with the gate oxide film. If the doping level of the gate electrode is light, a depletion region also grows in the poly-silicon gate electrode from the interface with the gate oxide film.

The thus-formed depletion region acts as an insulator region, increasing the gate oxide breakdown (durable) voltage. As a result, even if the gate oxide film is thin, the gate electrode having the depletion region can withstand a higher voltage. The invention defined by the independent claims provides high voltage CMOS doped at a low impurity concentration to provide enhanced gate oxide breakdown voltage, while also providing the lower voltage CMOS at a higher impurity concentration.

In particular, claim 20 is directed to a method of manufacturing a semiconductor device. The method comprises: (a) doping an active region and gate electrode of a high voltage CMOS circuit at a low impurity concentration; and (b) doping an active region and gate electrode of a low voltage CMOS circuit at a high impurity concentration after the step (a), to provide a high voltage CMOS circuit having enhanced gate oxide breakdown voltage due to a lightly doped gate electrode relative to the low voltage CMOS circuit.

In the rejection of claim 20 based on Hidaka, the Examiner again took the position that the claimed features were shown in ***all*** of the figures of Hidaka, including the prior art, and related text. The Examiner was somewhat more specific in referring to Column 8, lines 15-67 of Hidaka, which appears to have been relied upon for the recited doping of a low voltage CMOS circuit at a high impurity concentration.

As was pointed out in the last response, there is no such description in column 8. Column 8 of Hidaka does show that the well contact regions 14b and 16b are heavily doped p^+ or N^+. However, to set forth a prima facie case of anticipation, each and every limitation of the claim must be clearly taught in the single reference cited, and the relationship between the elements must be the same. Column 8 of Hidaka contains no teaching whatsoever of:

> (a) doping an active region and gate electrode of a high voltage CMOS circuit at a low impurity concentration; and
>
> (b) doping an active region and gate electrode of a low voltage CMOS circuit at a high impurity concentration after said step (a) . . . .

In response to Applicant having pointed out this fact in the last response, the Examiner, in the "Response to Arguments" section of the Office Action dated March 21, 2005, said that, based on the teaching of a second reference, Kim et al., it is clear that Hidaka "implicitly" possesses this limitation. The reasoning utilized was that "in order to make a memory device having a memory region and a peripheral region it is imperative to have a low voltage (i.e., low impurity concentration) region and a high voltage (i.e., high impurity concentration) region."

However, even if this were true (and no admission is being made that it is), this is ***not what is being recited.*** What is being recited in claim 20 is high impurity for a low voltage region and low impurity for a high voltage region--*the opposite of what the Examiner says Kim et al., and allegedly Hidaka, teaches.* That is, the prior art is alleged by the Examiner to teach high impurity with high voltage and low impurity with low voltage. On the other hand, what

is actually recited in claim 20 is low impurity with high voltage and high impurity with low voltage.

Thus, even if, for purposes of argument, Hidaka showed what the Examiner alleged in the Response to Arguments (and no admission is made to this effect), it would teach something quite different from what is recited feature of claim 20. For at least this reason, no prima facie case of anticipation has been set forth, and claim 20 is believed patentable over Hidaka.

Claim 9 recites, inter alia, (e) doping the first active region and the first gate electrode with an impurity of the second conductivity type to form a first transistor driven at a first voltage level, the first gate electrode being doped at a first concentration and (f) doping the second active region and the second gate electrode with an impurity of the second conductivity type to form a second transistor to be driven at a second voltage level lower than the first voltage level, the second gate electrode being doped at a second concentration higher than the first concentration.

Independent claim 9 was rejected in view of Hidaka and Mogami. The Examiner relied upon Hidaka, at column 8, lines 38-50 regarding steps (e) and (f). However, even if Hidaka teaches what it is alleged to "implicitly" teach in the Response to Arguments, it in no way teaches steps (e) and (f), which have a lower (first) impurity concentration for the first transistor to be driven at a higher (first) voltage level and a higher (second) impurity concentration for the second transistor to be driven at the lower (second) voltage.

Again, this is the *opposite* of what the Examiner alleges that Hidaka "implicitly" teaches. Thus, even based on the Examiner's reasoning, Hidaka in no way supplies the feature of steps (e) and (f). For at least this reason, no prima facie case of obviousness has been set forth as against claim 9.

Mogami shows forming a gate electrode from undoped polysilicon layers, but does not remedy the deficiencies of Hidaka. For at least the above reasons, claim 9 is believed clearly patentable over the cited references.

The other claims in this application are each dependent from one or another of the independent claims discussed above and are therefore believed patentable for the same reasons. Since each dependent claim is also deemed to define an additional aspect of the invention, however, the individual reconsideration of the patentability of each on its own merits is respectfully requested.

It is respectfully requested that the Examiner contact Applicant's undersigned attorney to arrange a time for a telephone interview to discuss the above rejections before issuing a new Office Action. Applicant's undersigned attorney can be contacted at the telephone number listed below.

In view of the foregoing amendments and remarks, Applicant respectfully requests favorable reconsideration and early passage to issue of the present application.

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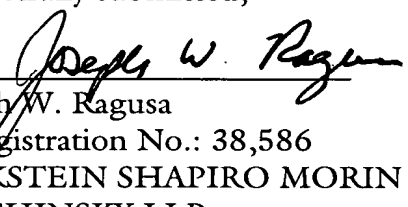
Respectfully submitted,

By 

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